ABSTRACT

An arithmetic block generates sum signal DVad and difference signal DVsu between the frames of image signals for every two frames from input image signal DVin. A bit rate proportion control block generates control signals CRad, CRsu for controlling the encoding bit rate proportion of the sum signal and the difference signal based on the sum signal DVad and the difference signal Dvsu. An encoding block generates encoded signal DTad with the encoding bit rate based on control signal CRad from the sum signal DVad using encoding process wherein the encoding bit rate can be altered on the basis of the control signals CRad. An encoding block also generates encoded signal DTsu with the encoding bit rate based on control signal CRsu from the difference signal DVsu.